Remarks

Applicants respectfully request reconsideration of this application as amended. No claims have been amended. No claims have been cancelled. Therefore, claims 1-28 are presented for examination.

Claims 1-4, 6-19, 21-24, 26-30 (as renumbered) stand rejected under 35 U.S.C. §103(a) as being unpatentable over Morris (U.S. Patent No. 5,859,999) in view of Poplingher (U.S. Patent No. 6,871,275). Applicants submit that Poplingher may not be considered as prior art precluding patentability of the present application.

Section 103(c) states that:

> *Subject matter developed by another person, which qualifies as prior art only under one or more of the subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.*

Poplingher is considered prior art under 35 U.S.C. §102(e) because it was filed prior to the filing of the present application, but was issued after the filing of the present application (effective filing date: 12-28-1999). Additionally, at the time of conception of the present application, the Poplingher reference and the application were both subject to an obligation of assignment to Intel Corporation. Therefore, due to the §102(e) status, and in light of §103(c), Poplingher cannot be used as a reference to preclude the patentability of claims 1-4, 6-19, 21-24, 26-30 under 35 U.S.C §103. Applicants respectfully request the withdrawal of the rejection of the claims under 35 U.S.C. §103 in view of Morris and

Poplingher since Morris alone does not preclude the patentability of claims 1-4, 6-19, 21-24, 26-30.

Claims 10 and 12-16 (as renumbered) stand rejected under 35 U.S.C. §103(a) as being unpatentable over Morris in view of Beckert (U.S. Patent No. 6,499,078). Applicants submit that the present claims are patentable over Morris in view of Beckert.

Morris discloses a method and apparatus for restoring a predicate register set. One embodiment includes decoding a first instruction which specifies a restoring operation to be performed on a predicate register set. In response to the first instruction, a mask is used to select a plurality of the predicate registers that are to be restored. The mask of the present invention consists of a first set of bits, with each bit of the first set of bits corresponding to a register in the predicate register set. When a bit of the first set of bits is set to one, the predicate register corresponding to that bit is restored. The mask further includes one bit corresponding to a plurality of registers in the predicate register set, wherein when that bit is set to one, the plurality of registers corresponding to that bit are restored. See Morris at Abstract.

Beckert discloses a hardware-implemented interrupt handler external to a processor handles interrupts destined for the processor. The interrupt handler has a programmable prioritized interrupt array with programmable registers that identify priority levels and handling processes for handling one or more interrupts. The interrupt handler also has an interrupt scanning state machine that scans the prioritized interrupt following receipt of an interrupt to extract the priority level and handling process associated with the interrupt. The interrupt handler is designed to handle interrupts in significantly less time than software

implementations, thereby making the handler favorable for real time systems. See Beckert at Abstract.

Claim 10 of the present application recites a processor abstraction layer including a plurality of interrupt handlers, each of the interrupt handlers further including saving architecture state code, the saving architecture state code further including a plurality of predefined sections. Applicants submit that neither Morris nor Beckert disclose or suggest interrupt handlers including saving architecture state code having a plurality of predefined sections. Therefore, claim 11 is patentable over Morris in view of Beckert since any combination of Morris and Beckert would fail to disclose or suggest such a feature.

Claims 11-16 depend upon and include the limitations of claim 10. Therefore, the combination of Morris and Miu also fails to render claims 11-16 obvious under 35 U.S.C. §103(a).

Claim 11 (originally claim 12) stands rejected under 35 U.S.C. §103(a) as being unpatentable over Morris and Beckert as applied to claim 10 above, and further in view of Miu (U.S. Patent No. 4,484,271). Applicants submit that the present claims are patentable over Morris and Beckert in view of Miu.

Miu discloses a hardware interrupt apparatus. See Miu at Abstract. Nonetheless, Miu does not disclose or suggest interrupt handlers including saving architecture state code having a plurality of predefined sections. As discussed above, both Morris and Beckert fail to disclose or suggest interrupt handlers including saving architecture state code having a plurality of predefined sections. Thus, any combination of Morris, Beckert and Miu would also not disclose or suggest the feature. As a result the present claims are patentable over the combination of Morris, Beckert and Miu.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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